1. (currently amended) An apparatus within a pipelined microprocessor for forwarding store instruction results to a pipeline stage for execution of a load instruction, the apparatus comprising:

a result forwarding cache (RFC), for storing at least one non-store instruction result destined for a user-visible register of the microprocessor, and for storing a plurality of store instruction results;

comparison logic, for comparing a load address of the load instruction with a plurality of store addresses associated with said plurality of store instruction results to generate an address match signal; and

control logic, configured to receive said match signal and selectively forward one of said plurality of store instruction results from said RFC to the pipeline stage in response to said match signal.

10. (currently amended) An apparatus for forwarding storehit data within stages of a pipelined microprocessor, the apparatus comprising:

a result forwarding cache (RFC), configured to forward at least one non-store instruction result, and to forward a first plurality of store instruction results;

a data unit, configured to forward a second plurality of store instruction results; and

selection logic, coupled to said RFC and said data unit, for selectively providing one of said first and second plurality of store instruction results to a stage of the microprocessor pipeline executing a load instruction.

18. (currently amended) An apparatus for detecting storehit conditions in a pipelined microprocessor in a hierarchical manner, the apparatus comprising:

first comparison logic, for comparing a load instruction load address in a first stage of the pipeline with a first plurality of store addresses of first store instruction data in a plurality of stages of the pipeline subsequent to said first pipeline stage, wherein said plurality of stages of the pipeline subsequent to said first pipeline stage do not comprise store buffers;

second comparison logic, for comparing said load address with a second plurality of store addresses of second store instruction data in a plurality of store buffers of the microprocessor; and

control logic, coupled to said first and second comparison logic, configured to determine which of said first and second store instruction data is newest based on said first and second comparison logic comparing.

21. (currently amended) An apparatus for speculatively forwarding storehit data in a microprocessor pipeline, the apparatus comprising:

a plurality of virtual address comparators, for comparing a virtual load address with a plurality of virtual store addresses to generate a virtual match signal;

a plurality of physical address comparators, for comparing a physical load address translated from said virtual load address with a plurality of physical store addresses translated from said plurality of virtual store addresses to generate a physical match signal;

forwarding logic, coupled to receive said virtual match signal, for forwarding the storehit data in response to said virtual match signal indicating no match between said virtual load address and said plurality of virtual store addresses, prior to generation of said physical match signal; and

control logic, for receiving said virtual and physical match signals and generating a stall signal for stalling the pipeline subsequent to said forwarding logic forwarding said storehit data if said physical match signal indicates a match between said physical load address and one of said plurality of physical store addresses but said virtual match signal indicates no match between said virtual load address and one of said plurality of virtual store addresses.

23. (currently amended) A pipelined microprocessor for speculatively forwarding storehit data from a first pipeline stage to a second pipeline stage, wherein the storehit data is specified by a load address in the second stage, comprising:

address region logic, configured to receive the load address and generate a match signal to indicate whether the load address is within one of a plurality of non-cacheable address regions of the microprocessor address space stored therein;

forwarding logic, for forwarding the storehit data from the first stage to the second stage ~~during a first clock cycle~~ prior to said address region logic generating said match signal; and

control logic, configured to receive said match signal and to assert a stall signal ~~during a second clock cycle~~, subsequent to said forwarding logic forwarding the storehit data, to stall the pipeline if said address region logic indicates the load address is within one of said plurality of non-cacheable address regions.

26. (currently amended) A method for forwarding storehit data in a microprocessor pipeline, the method comprising:

storing at least one store instruction result and at least one non-store instruction result into a result forwarding cache of the microprocessor;

detecting a storehit condition, wherein a load instruction in a stage of the pipeline specifies data generated by a previous store instruction, wherein said data is still present in the pipeline;

determining whether said data is present in ~~a~~ said result forwarding cache ~~of the microprocessor~~;

selectively forwarding said data from said result forwarding cache to said stage if said data is in said result forwarding cache; and

selectively forwarding said data from a data unit of the microprocessor to said stage if said data is not in said result forwarding cache.

30. (currently amended) A method for speculatively forwarding storehit data in a microprocessor pipeline, the method comprising:

determining that a virtual load address matches no virtual store addresses present in the pipeline;

~~speculatively~~ forwarding storehit data from a first stage to a second stage of the pipeline based on ~~a virtual address comparison between a load address and a plurality of store addresses~~ said determining that said virtual load address matches no virtual store addresses present in the pipeline;

detecting that a physical load address translated from said virtual load address matches a physical store address present in the pipeline, subsequent to said forwarding said storehit data; and

~~detecting a virtual aliasing condition with respect to said load address and one of said plurality of store addresses based on a physical address comparison between said load address and said plurality of store addresses after said speculatively forwarding;~~ and

stalling the pipeline in response to said detecting that said physical load address translated from said virtual load address matches said physical store address present in the pipeline~~said virtual aliasing condition~~.

32. (canceled)

34. (currently amended) A method for speculatively forwarding storehit data in a microprocessor pipeline, the method comprising:

detecting a storehit condition by comparing a load address with a plurality of store addresses;

~~speculatively~~ forwarding storehit data in response to said detecting said storehit condition;

determining said load address is within a non-cacheable address region subsequent to said speculatively forwarding; and

stalling the pipeline in response to said determining said load address is within a non-cacheable address region.